Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	(cobalt with (erasable adj programmable adj read adj only adj memory))	US-PGPUB; USPAT	OR	ON	2005/06/15 09:50
L2	0	(cobalt same (erasable adj programmable adj read adj only adj memory))	US-PGPUB; USPAT	OR	ON	2005/06/15 09:26
L3	0	(cobalt same (erasable adj programmable adj read adj only adj memory))	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 09:27
L4	0	(cobalt same (EPROM))	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 09:28
L5	5	(cobalt same (EPROM))	US-PGPUB; USPAT	OR	ON	2005/06/15 09:47
L6	4	5 and titanium	US-PGPUB; USPAT	OR	ON	2005/06/15 09:28
L7	467	cobalt and EPROM	US-PGPUB; USPAT	OR	ON	2005/06/15 09:47
L8	4	7 and (titanium same ionized)	US-PGPUB; USPAT	OR	ON	2005/06/15 09:50
L9	450	cobalt and (erasable adj programmable adj read adj only adj memory)	US-PGPUB; USPAT	OR	ON	2005/06/15 09:50
L10	2	9 and (titanium same ionized)	US-PGPUB; USPAT	OR	ON	2005/06/15 10:00
L13	3112	438/533,583,586,649,655,664, 682,683.ccls.	US-PGPUB; USPAT	OR	ON	2005/06/15 10:27
L14	2619	13 and @ad<"20020123"	US-PGPUB; USPAT	OR	ON	2005/06/15 10:28
L15	731	14 and cobalt and titanium	US-PGPUB; USPAT	OR	ON	2005/06/15 10:28
L16	722	15 and silicide	US-PGPUB; USPAT	OR	ON	2005/06/15 10:28
L17	1322	257/754,755,757,768,769.ccls.	US-PGPUB; USPAT	OR	ON	2005/06/15 10:27
L18	1176	17 and @ad<"20020123"	US-PGPUB; USPAT	OR	ON	2005/06/15 10:28
L19	814	18 and silicide	US-PGPUB; USPAT	OR	ON	2005/06/15 10:28
L20	173	19 and cobalt and titanium	US-PGPUB; USPAT	OR	ON	2005/06/15 10:28

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	(cobalt with (erasable adj programmable adj read adj only adj memory))	US-PGPUB; USPAT	OR	ON	2005/06/15 09:50
L2	0	(cobalt same (erasable adj programmable adj read adj only adj memory))	US-PGPUB; USPAT	OR	ON	2005/06/15 09:26
L3	0	(cobalt same (erasable adj programmable adj read adj only adj memory))	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 09:27
L4	0	(cobalt same (EPROM))	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 09:28
L5	5	(cobalt same (EPROM))	US-PGPUB; USPAT	OR	ON	2005/06/15 09:47
L6	4	5 and titanium	US-PGPUB; USPAT	OR	ON	2005/06/15 09:28
L7	467	cobalt and EPROM	US-PGPUB; USPAT	OR	ON	2005/06/15 09:47
L8	4	7 and (titanium same ionized)	US-PGPUB; USPAT	OR	ON	2005/06/15 09:50
L9	450	cobalt and (erasable adj programmable adj read adj only adj memory)	US-PGPUB; USPAT	OR	ON	2005/06/15 09:50
L10	2	9 and (titanium same ionized)	US-PGPUB; USPAT	OR	ON	2005/06/15 09:50

US-PAT-NO: 6815781

DOCUMENT-IDENTIFIER: US 6815781 B2

TITLE: Inverted staggered thin film transistor with salicided source/drain structures and method of making same

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Detailed Description Text - DETX (12):

The polysilicon layer 17 that makes up a portion of the source 13 and drain 15 electrodes preferably comprises a heavily doped polysilicon layer of the first conductivity type. The metal silicide layer 19 that makes up the other portion of the source 13 and drain 15 electrodes preferably comprises a **cobalt** silicide layer. Alternatively, layer 19 may comprise other silicide layers, such as a titanium silicide or nickel silicide layer. While the source 13 and drain 15 electrodes have been described as comprising two layers 17 and 19, additional layers and materials may be added to these electrodes 13 and 15, if desired.

Detailed Description Text - DETX (13):

As discussed above, in a preferred aspect of the present invention, the inverted staggered thin film transistor 1 preferably contains a charge storage region and is used in a memory device, such as in an **erasable programmable read only memory** (EPROM) or in an electrically **erasable programmable read only memory** (EEPROM). In this case, the transistor source and drain electrodes or lines are referred to as bit lines and the gate electrode or line is referred to as a word line. Preferably, the gate electrode 3 comprises a portion of a gate line that extends below the source 23 and drain 25 regions in the direction parallel to the source 23 to drain 25 direction. Preferably, the source 13 and drain 15 electrodes comprise portions of respective bit lines that extend perpendicular to the source 23 to drain 25 direction.

Detailed Description Text - DETX (36):

A method of making the inverted staggered thin film transistors of the preferred embodiments shown in FIGS. 1-3 will now be described. A gate electrode 3 is formed over a substrate. For example, the gate electrode may comprise a first heavily doped polysilicon layer 27 over a **titanium/titanium** nitride film 29 over a second heavily doped polysilicon layer 26. Preferably, layer 27 is about 2000 to 3000 Angstroms thick and layer 26 is about 1000 to

3000 Angstroms thick. Layers 27 and 26 are preferably heavily P-type doped to a concentration of 1.times.10.sup.19 to 5.times.10.sup.21 cm.sup.-3, preferably 1.times.10.sup.20 to 5.times.10.sup.21 cm.sup.-3. Layers 27 and 26 may be doped in situ during deposition or by ion implantation after deposition. The **titanium** layer may be about 100 to 500 Angstroms thick **titanium** layer deposited by physical vapor deposition (PVD) or **ionized** metal plasma PVD (IMP-PVD). The **titanium** nitride layer may be an about 100 to 200 Angstrom TiN layer deposited by PVD, IMP-PVD or metal organic chemical vapor deposition (MOCVD). However, any other suitable materials, deposition methods and layer thickness may be used instead. Preferably, the **titanium** layer reacts with the lower polysilicon layer 26 during a subsequent anneal to form a **titanium** silicide layer.

Detailed Description Text - DETX (41):

To form the transistor 1 of the first preferred embodiment, a metal layer 51 is formed in the openings 11 and over a top surface of the fill layer 9, as shown in FIG. 7. The metal layer 51 may be any layer which forms a metal suicide layer when it reacts with silicon. Preferably, metal layer 51 comprises a **cobalt,** titanium or nickel layer. The metal layer 51 may have any suitable thickness that can form a metal silicide layer by reaction with a portion of the polysilicon active layer 7 without converting the entire thickness of the active layer 7 to metal silicide. Thus, the thickness of the metal silicide layer 51 is preferably proportional to the thickness of the active layer 7. For example, layer 51 may comprise a 20 to 300 Angstrom, preferably 50 to 100 Angstrom thick **cobalt** layer deposited by physical vapor deposition, such as by the IMP-PVD method.

Claims Text - CLTX (9):

9. The device of claim 8, wherein: the charge storage region comprises: a dielectric isolated floating gate; an insulating layer containing conductive nanocrystals; or a composite dielectric film comprising a tunneling layer, a charge storage layer and a blocking dielectric layer; the active layer comprises a polysilicon active layer; the insulating fill layer comprises silicon dioxide; and the metal silicide layer comprises a titanium silicide layer, a **cobalt** silicide layer or a nickel silicide layer.

Other Reference Publication - OREF (2):

Thermal Stability of **Cobalt** and Nickel Silicides in Amorpho Crystalline Silicon, Abstract of M.C. Poon, IEDM 1997 Prtoc. p. 19.